**Abstract**

Switching times of a thyristor-based semiconductor device are improved by enhancing carrier drainage from a buried thyristor-emitter region. According to an example embodiment of the present invention, a conductive contact extends to a doped well region buried in a substrate and is adapted to drain carriers therefrom. The device includes a thyristor body having at least one doped emitter region buried in the doped well region. A conductive thyristor control port is adapted to capacitively couple to the thyristor body and to control current flow therein. With this approach, the thyristor can be rapidly switched between resistance states, which has been found to be particularly useful in high-speed data latching implementations including but not limited to memory cell applications.